REMARKS

1-3. Claim 1 stands rejected as anticipated by Wilson under 35 U.S.C. §102(b). The office action states:

> 3. Regarding claim 1, Wilkinson taught a method for simultaneous processing of information (column 3, lines 23-29) comprising:
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> providing a matrix comprising a plurality of cells (column 6, lines 52-61), each cell of the plurality of cells comprising at least one processor and at least one page (column 24, lines 30-36), the at least one page comprising one selected from the set consisting of format counters, data pointers and processor counters (column 26, lines 40-46);
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> connecting at least one cell to at least one area of random access memory, the area comprising at least one addressable location (column 28, lines 59-64), and the connection being dynamically re-allocable to at least a second area of random access memory (column 28, lines 20-24; column 28, line 64 - column 29, line 7);
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> locating instructions and registers in random access memory areas (column 26, lines 59-66); and processing information by at least one of the plurality of cells executing instructions pointed to by at least one process counter (column 24, lines 30-36, column 27, lines 58-62). Pp.2-3.

This ground of rejection is respectfully traversed. "It is well settled that anticipation under 35 U.S.C. 102 requires the presence in a single reference of all of the elements of a claimed invention." *Ex parte Chopra*, 229 U.S.P.Q. 230, 231 (BPA&I 1985) and cases cited.

"Anticipation requires the presence in a single prior art disclosure of all elements of a claimed invention arranged as in the claim." *Connell v. Sears, Roebuck & Co.*, 220 U.S.P.Q. 193, 198 (Fed. Cir. 1983).

"This court has repeatedly stated that the defense of lack of novelty (i.e., 'anticipation') can only be established by a single prior art reference which discloses each and every element of the claimed invention." *Structural Rubber Prod. Co. v. Park Rubber Co.*, 223 U.S.P.Q. 1264, 1270 (Fed. Cir. 1984), citing five prior Federal Circuit decisions since 1983 including *Connell.*

In a later analogous case the Court of Appeals for the Federal Circuit again applied this rule in reversing a denial of a motion for judgment n.o.v. after a jury finding that claims were anticipated. *Jamesbury Corp. v. Litton Industrial Prod., Inc.*, 225 U.S.P.Q. 253 (Fed. Cir. 1985).

After quoting from *Connell*, "Anticipation requires the presence in a single prior art disclosure of all elements of a claimed invention arranged as in the claim," 225 U.S.P.Q. at 256, the court observed that the patentee accomplished a constant tight contact in a ball valve by a lip on the seal or ring which interferes with the placement of the ball. The lip protruded into the area where the ball will be placed and was thus deflected after the ball was assembled into the valve. Because of this constant pressure, the patented valve was described as providing a particularly good seal when regulating a low pressure stream. The court quoted with approval from a 1967 Court of Claims decision adopting the opinion of then Commissioner and later Judge Donald E. Lane:

> [T]he term "engaging the ball" recited in claims 7 and 8 means that the lip contacts the ball with sufficient force to provide a fluid tight seal. *** The Saunders flange or lip only sealingly engages the ball 1 on the upstream side when the fluid pressure forces the lip against the ball and never sealingly engages the ball on the downstream side because there is no fluid pressure there to force the lip against the ball. The Saunders sealing ring provides a compression type of seal which depends upon the ball pressing into the material of the ring. *** The seal of Saunders depends primarily on the contact between the ball and the body of the sealing ring, and the flange or lip sealingly contacts the ball on the upstream side when the fluid pressure increases. 225 U.S.P.Q. at 258.

Relying on *Jamesbury*, the ITC said, "Anticipation requires looking at a reference, and comparing the disclosure of the reference with the claims of the patent in suit. A claimed device is anticipated if a single prior art reference discloses all the elements of the claimed invention as arranged in the claim." *In re Certain Floppy Disk Drives and Components Thereof*, 227 U.S.P.Q. 982, 985 (U.S. ITC 1985).

To allegedly anticipate providing a matrix comprising a plurality of cells with each cell of the plurality of cells comprising at least one processor and at least one page with the at least one page comprising one selected from the set consisting of format counters, data pointers and process counters, the office action jumps from column six to column 24 and then to column 26.

The plurality of cells is said to be found in column 6 lines 52-61 which reads as follows:

> Generally, a node is the junction of links. In a generic array of PE's one PE can be a node. A node can also contain a collection of PE's called a module.

> In accordance with our invention a node is formed of an array of PME's , and we refer to the set of PME's as a node. Preferably a node is 8 PME's.
>
> Node Array
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> A collection of modules made up of MME's is sometimes referred to as a node array, is an array of nodes made up of modules. A node array is usually more than a few PME's, but the term encompasses a plurality.

This portion is not a matrix of cells as exemplified in the paragraph beginning at line 18 of page 9 of the specification.

The office action jumps to column 24, lines 30-36 for what is said to be a disclosure of each cell comprising at least one processor and at least one page. This portion reads:

> The PME's are self-contained stored program microcomputers comprising a main store, local store, operation decode, arithmetic /logic unit (ALU), working registers and Input/Output I/O ports. The PME's have the capability of fetching and executing stored instructions form their own main store in MIMD operation or to fetch and execute commands via the BCI interface in SIMD mode.

But that is not a disclosure of the page disclosed in this application in the last paragraph on page three of the specification that contained definitions of the information, automate the get function for getting information and automate the analysis of the information that is collected.

The office action then refers to column 26 lines 40-46 as disclosing a page selected from the set consisting of format counters, data pointers and processor counters. But that portion reads:

> The important paths of the internal data flows use 12 nanosecond hard registers such as the OP register 450, M register 440, WR register 470, and the program counter PC register 430. These registers feed the fully distributed ALU 460 and I/O router registers and logic 405, 406, 407, 408 for all operations.

Manifestly, that portion does not modify anything resembling the nonexistent pages said to be present in column 26 lines 30-36.

The office action then cites the passage at column 28, lines 59-64 as disclosing connecting at least one cell to at least one area of random access memory, the area comprising at least one addressable location. But this passage reads:

> As seen in FIG. 7 and 8 Data on a PME input port may be destined for the local PME, or for a PME further down the ring. Data destined for a PME further down the ring may be stored in the local PME main memory and then forwarded by the local PME towards the target PME (store and forward), or the local imput port may be logically connected to a particular local output port (circuit switched) such that the data passes "transparently" through the local PME on its way to the target PME.

That is hardly a disclosure of connecting the at least one cell to at least one area of random access memory.

The office action continues by referring to column 28, lines 20-24 and column 28, line 64-column 29, line 7 as disclosing the connection being dynamically re-allocable to at least a second area of random access memory. But those passages read:

> Input ports are connected such that data may be routed from input to memory or from input AR register 405 to output register 408 via direct 16 bit data path 425. Memory would be the data sink for messages targeting at the PME or for messages that were moved in 'store and forward' mode. Column 28, lines 19-24.
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> forward), or the local input port may be logically connected to a particular local output port (circuit switched) such that the data passes "transparently" through the local PME on its way to the target PME. Local PME software dynamically controls whether or not the local PME is in "store and forward" mode or in "circuit switched" mode for any of the four inputs and four outputs. In circuit switched mode, the PME concurrently processes all functions except the I/O associated with the circuit switch; in store and forward mode the PME suspends all other processing functions to begin the I/O forwarding process. Column 28, line 64-column 29, line 7.

The office action refers to the passage at column 26, lines 59-66 as disclosing locating instructions and registers in random access memory areas. But that passage reads:

> The PME data flow consists of a 16 word by 16 bit general register stack, a multi-function arithmetic/logic unit (ALU) working registers to buffer memory addresses, memory output registers, ALU output registers, operation/command, I/O output registers, and multiplexers to select inputs to the ALU and registers. Current CMOS VLSI technology for 4 MByte DRAM memory with our logic permits a PME to execute instruction steps at 25 Mhz.

But that passage only discloses a number of registers, not locating instructions and registers in random access memory areas.

Finally the office action cites column 24, lines 30-36 and column 27, lines 58-62 as disclosing processing information by at least one of the plurality of cells executing instructions pointed to by at least one process counter.

But those passages read:

> The PME's are self-contained stored program microcomputers comprising a main store, local store, operation decode, arithmetic/logic unit (ALU), working registers and Input/Output I/O ports. The PME's have the capability have the capability of fetching and executing sored instructions form their own main store in MIMD operation or to fetch and execute commands via the BCI interface in SIMD mode. Column 24, lines 30-36.

> In MIMD mode the PME maintains a program counter PC address and uses that as the address within its own memory to fetch a 16 bit instruction. Instruction decode and execution proceeds as in most any other RISC type machine. Column 27, lines 58-62.

That is hardly a disclosure of processing information that at least one of the plurality of cells executing instructions pointed to by at least one process counter.

Accordingly, withdrawal of the rejection of the claim as anticipated by this reference is respectfully requested.

4,5. Claim 1 also stands rejected under 35 U.S.C. §102(e) as being anticipated by Pincus. The office action states:

> 5. Regarding claim 1, Pincus taught a method for simultaneous processing of information (column 3, lines 45-55) comprising:
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> providing a matrix comprising a plurality of cells (column 9, lines 33-39), each cell of the plurality of cells comprising at least one processor and at least one page, the at least one page comprising one selected from the set consisting of format counters, data pointers and processor counters (column 10, line 59 - column 11, line 9);
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> connecting at least one cell to at least one area of random access memory, the area comprising at least one addressable location (column 12, lines 6-16, 35-40), and the connection being dynamically re-allocable to at least a second area of random access memory (column 13, lines 1-13);

> locating instructions and registers in random access memory areas (column 15, lines 20-37); and
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> processing information by at least one of the plurality of cells executing instructions pointed to by at least one process counter (column 15, lines 48-56). P.3.

The office action refers to column 9, lines 33-39 as disclosing a matrix comprising a plurality of cells. This passage reads:

> FIG. 3 illustrates an aspect of the present invention in a multiple processor, single bi-directional bus system. Multiple processing elements 40, I/O interface 10 and memory 14 are connected to bus 16. Sequencer 24 includes an array of CPU (i.e. processor) registers that are manipulated by the processing elements on the bus based on whether they are requesting, using or releasing data bus 16.

That is hardly a disclosure of a matrix comprising a plurality of cells as disclosed in this application.

The office action identifies column 10, line 59-column 11, line 9 as disclosing each cell as comprising at least one processor and at least one page with the at least one page comprising one selected from the set consisting of format counters, data pointers and processor counters. That passage reads:

> Referring now to FIGS. 6A and 6B, which together constitue an overall block diagram of a preferred embodiment of a matrix processor 26, interface bus 42 from main computer 28 is coupled to interface processor (IFP) 44. Register/control address lines 46 then connect between the interface processor and each of a first high performance parallel interface (HIPPI block 48, a second high performance parallel interface (HIPPI) block 50, arbitrator block 52, processor nodes 2 & 3 shown as block 54, processor nodes 4 & 5 shown as block 56 and processor nodes 6 & 7 shown as block 58. Register/control data bus 60 supplies data to each of block 62 (which corresponds to memory 37 in FIG. 5). The various registers of the system are memory mapped to reside within the register control address space which suitably comprises the "lower half" of addressable memory of the matrix processor in the perferrred embodiment.

That is not a disclosure of a nonexistent cell comprising both at least one processor and at least one page comprising one selected from the set consisting of undisclosed format counters, data pointers and processor counters.

The office action continues in citing column 12, lines 6-16 and 35-40 as disclosing connecting at least one cell to at least one area of random access memory comprising at least one addressable location. These passages read:

> Busses 84 and 86 may transfer data to and from memory 62 through the interfaces 48 and 50. When data is transferred into the matrix processor either interface 48 or 50 provides the address over P0ADDR bus 68 through arbitrator 52 to memory 62. Data is transferred from memory 62 over P0DATA bus 64 through the requesting parallel interface processor and transmitted over data bus 86 or 84 respectively to an external device. When data is transferred between the processing nodes and memory 62 the data is sent directly to memory 62 while the address is first processed by arbitrator 52 before being sent to the memory.
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> ...
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> The address and control signals are decoded by logic circuit 90 while output of the logic circuit is provided to the CPU register array 88. Register control address bus 46 is also decoded by decode logic circuit 90, and register control data bus 60 is coupled to CPU register array 88 as well as to the processing element data lines.

That is not a disclosure of connecting the nonexistent cell to an area of random access memory.

The office action continues, relying on column 13, lines 1-13 as disclosing the connection being re-allocable to at least a secondary of random access memory. That passage reads:

> When a processor node lowers the PnLOCK* signal it is given access to all memory ports and normal arbitration for all other nodes is disabled as described in conjunction with FIGS. 13A and 13B herein. The PnWRITE signal identifies write accesses (if PnWRITE is asserted) or read access (if PnWRITE is not asserted) of memory. Port interface logic block 89 contains logic for generating the request for memory reads and writes asserting the PnMREQ signal when a CPU on the node wishes to access memory via the crossbar. PnWRITE is asserted if the access is write, or deasseerted if the access is to be a read access.

That is not a disclosure of a connection being dynamically re-allocable to at least a secondary of random access memory.

The office action continues by citing column 15, lines 20-37 as disclosing locating instructions and registers in random access memory areas. That passage reads:

> Core execution unit 100, comprising instruction sequencer 102, integer ALU 104 and integer register array 106, controls overall operation of the processing element. The address bus 108 and code bus 110 of sequencer 102 are coupled to code cache 94 while the address bus 112 of integer register array 106 is fed to translation lookaside buffer 92 as well as data cache 96. Data cache 96 supplies data to register array 106 and floating point register array 98 via data bus 114. The input and output of integer ALU 104 are coupled to register array 106, while the input and output of a floating point multiplier 116 and a floating point adder 118 are connected to floating point register array 98. Translation lookaside buffer 92 transmits data to data cache 96 or data bus 66, and instructions to code cache 94 or address bus 70. Code cache 94 transfers instructions to sequencer 102 after the sequencer 102 transmits the appropriate address, sequencer 102 controlling integer branches and control instructions for the processing element.

That is not a disclosure of locating instructions and registers in random access memory areas.

Finally, the office action concludes by citing column 15, lines 48-56 as disclosing processing information by at least one of the plurality of cells executing instructions pointed to by at least one process counter. That passage reads:

> Initial instructions for each data processing unit are transferred from memory block 62 (FIG. 6B) into code cache 94. After the algorithm is loaded into code cache 94, a block of data array stored in memory 62 is also transferred into data cache 96. The CPU then releases data bus 66 and address/control bus 70 by setting and clearing the appropriate CPU registers 88 (FIG. 7) and the CPU begins to perform the algorithm loaded into the code cache with the data block loaded into the data cache. During the internal processing of the data block, other CPUs are free to use buses 66 and 70.

That is not a disclosure of processing information by at least one of the nonexistent cells executing instructions that are not pointed to by any process counter.

Accordingly, withdrawal of the rejection of claim 1 as anticipated by this reference is respectfully requested.

While the Examiner has identified particular passages in the references, the references do not use the terminology in the claims. They disclose processes functionally quite different from the invention disclosed and claim in this application. Accordingly, if this ground of rejection is repeated, the Examiner is respectfully requested to quote verbatim the language in each reference he regards as corresponding to at least "a cell, a format counter, a data pointer and process counter."

The courtesy of the Examiner in conducting a diligent search is acknowledged with appreciation. The references cited but not applied are evidently less likely than the references cited to anticipate, suggest or make obvious the subject matter as a whole of the invention disclosed and claimed in this application.

In view of the forgoing authorities, remarks and the inability of the prior art to anticipate, suggest or make obvious the subject matter as a whole of the invention disclosed and claimed in this application, this application is submitted to be in a condition for allowance, and notice thereof is respectfully requested.

Enclosed is a $60 check for the Petition for Extension of Time fee. Please apply any other charges or credits to deposit account 06-1050, Order No. 03243-010001.

Respectfully submitted,
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Date: JUL 2 5 2005

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